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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,354	07/07/2003	Thomas J. Sonderman	2000.100800	7900

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,354	THOMAS J. SONDERMAN	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1 and 16 are objected to because of the following informalities: In claims 1 and 16, line 5, after "said at", delete "lest" and insert --least--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kline (U.S. Pub. 2003/0129775).

In re claims 1, 9, and 16, **Kline** discloses a method, comprising: performing at least one electrical test on at least one semiconductor device (page 2, paragraph [0012]); determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed semiconductor device (i.e., memory device, transistor...) based upon electrical data obtained from the at least one electrical test; and performing the at least one process operation comprised of the determined at least one parameter to form at least one gate insulation layer on the subsequently formed semiconductor device (page 2, paragraphs [0013]-[0014] and FIGS. 1-11).

In re claims 2 and 10, **Kline** discloses wherein the semiconductor device is at least one of a flash memory device, an application specific integrated circuit and a microprocessor (page 2, paragraph [0012]).

In re claims 3, 11, and 17, **Kline** discloses wherein performing the at least one electrical test on the at least one semiconductor device comprises performing the at least one electrical test on the at least one semiconductor device to determine at least one of a breakdown voltage, a threshold voltage, a state charge, an interface charge, a trapped charge, a surface charge, a programming cycle time and an erase cycle time (page 2, paragraph [0012]).

In re claim 4, **Kline** discloses wherein the semiconductor device is comprised of at least one transistor that is comprises of a gate insulation layer and a gate electrode positioned above the gate insulation layer (page 1, paragraph [0011]).

In re claims 5 and 12, **Kline** discloses wherein the semiconductor device is comprised of a memory device that is comprised of a gate insulation layer, a floating gate layer positioned above the gate insulation layer, an intermediate insulation layer positioned above the floating gate layer, and a control gate layer positioned above the intermediate insulation layer (page 2, paragraph [0011]).

In re claims 6, 13, and 18, **Kline** discloses wherein the at least one process operation is comprised of at least one of a deposition process and a thermal growth process (page 2, paragraph [0014]).

In re claims 7, 14, and 19, **Kline** discloses wherein at least one parameter is comprised of at least one of a temperature, a pressure, a duration, a process gas flow rate,

a process gas composition, a liquid flow rate, a liquid composition, and a power level setting (page 2, paragraph [0012]).

In re claims 8, 15, and 20, **Kline** discloses wherein the gate insulation layer is comprised of at least one of silicon dioxide and silicon nitride (page 3, paragraph [0013]).

2. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Kline (U.S. Pub. 2003/0129775).

In re claim 21, **Kline** discloses a method, comprising: performing at least one electrical test on at least one memory device to determine a duration of a programming cycle performed on the memory devices (page 2, paragraph [0012]); determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon the determined duration of the programming cycle; and performing the at least one process operation comprised of the determined at least one parameter to form at least one gate insulation layer on the subsequently formed memory device (page 2, paragraphs [0013]-[0014] and FIGS. 1-11).

3. Claim 22 is rejected under 35 U.S.C. 102(e) as being anticipated by Kline (U.S. Pub. 2003/0129775).

In re claim 22, **Kline** discloses a method, comprising: performing at least one electrical test on at least one memory device to determine a duration of an erase cycle performed on the memory devices (page 2, paragraph [0012]); determining at least one parameter of at least one process operation to be performed to form at least one gate insulation layer on a subsequently formed memory device based upon the determined

duration of the erase cycle; and performing the at least one process operation comprised of the determined at least one parameter to form at least one gate insulation layer on the subsequently formed memory device (page 2, paragraphs [0013]-[0014] and FIGS. 1-11).

Response to Applicant's Amendment and Arguments

Applicant's arguments filed September 20th, 2004 have been fully considered but they are not persuasive.

Applicants contend that Kline, U.S. Patent Application Publication No. US 2003/0129775 A1 Herein know as Kline fails to disclose or even remotely suggest the methodology whereby at least one parameter of a process operation to be performed to form an insulation layer on a subsequently formed device is based upon electrical test data obtained from a previous electrical test.

In response to Applicants' contention that Kline fails to disclose or even remotely suggest the methodology whereby at least one parameter of a process operation to be performed to form an insulation layer on a subsequently formed device is based upon electrical test data obtained from a previous electrical test, Examiner respectfully disagrees. Please note that Kline teaches a methodology addressing delays in transmission of electrical signals between chips are directly related to distances (paragraph [0004]). This is well known in the art as propagation delays. A preference parameter is inherent in Kline and without having a reference parameter in Kline, it would be difficult at best to determine a successful test of the electronic devices.

For these reasons, examiner holds the rejection proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
November 16th, 2004

W. David Coleman
Primary Examiner